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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,062	04/28/2005	Tadaaki Tanimoto	TAM-104	3125

24956 7590 08/19/2009

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EXAMINER	
SANDOVAL, PATRICK	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
08/19/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,062	TANIMOTO ET AL.	
	Examiner	Art Unit	
	PATRICK SANDOVAL	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to Applicant's amendment filed 5/19/2009. Claims 1 and 6 are amended, and claims 2-4 have been cancelled. Claims 1 and 6 are pending.

Response to Amendment

2. Applicant's arguments, see Remarks Pages 5-8, filed 5/19/2009, ***with respect to the rejection(s) of claim(s) 1-4 and 6*** under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

3. However, upon further consideration, a new ground(s) of rejection is made in view of previously applied prior art references Bowen (US 6,691,301), Panchul et al. (US2001/0034876), and Hines (2005/0246682), newly discovered prior art reference Curtis (US 2003/0051064), and IDS reference (Nakata) A. Nakata, et al., "Deriving Parameter Conditions for Periodic Timed Automata Satisfying Real-Time Temporal Logic Formulas", Proc. of IFIP TCPfWG6. 1 Int. Conf. on Formal Techniques for Networked and Distributed Systems (FORTE2001),Kluwer Academic Publishers, 2001.08, pages 151-166, which was previously submitted by Applicant for consideration on 4/28/2005.

Claim Objections

4. Claims 1 and 6 are objected to because the acronym "RPCTL" in the last line of claim 1 and the last line of claim 6 is not defined. Examiner suggests inserting --(Real-time Parametric Computation Tree Logic)-- following "RPCTL" in each respective claim, to correspond with Applicant's specification, Page 30, lines 6-7.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1 and 6 are rejected** under 35 U.S.C. 103(a) as being unpatentable over **Bowen** (US 6,691,301) in view of **Panchul** et al. (US2001/0034876), further in view of **Hines** (2005/0246682), further in view of **Curtis** (US 2003/0051064), further in view of **Nakata**, et al., (Nakata), "Deriving Parameter Conditions for Periodic Timed Automata Satisfying Real-Time Temporal Logic Formulas", Proc. of IFIP TCP/WG6. 1 Int. Conf. on Formal Techniques for Networked and Distributed Systems (FORTE2001), Kluwer Academic Publishers, 2001.08, pages 151-166.

7. **Pursuant to claims 1 and 6**, Bowen discloses:

inputting program descriptions which define a plurality of devices by employing a program language capable of describing parallel operations (Bowen, Col. 1, ll. 47-61, Col. 9, ll. 63-67 – Col. 10, ll. 1-43);

converting the input program descriptions into an intermediate expression (Bowen, Col. 44, ll. 25-55, compile Handel-C to VHDL);

generating parameters which satisfy a real-time restriction, for the intermediate expression (Bowen, Col. 9, ll. 55-67 – Col. 10, ll. 1-11, requirements, Col. 229, ll. 9-51, behavioral description and varying parameters);

synthesizing circuit descriptions which are based on a hardware description language (Bowen, Col. 44, ll. 25-55, compile Handel-C to VHDL, RTL synthesis), on the

basis of the generated parameters (Bowen, Col. 229, ll. 9-51, behavioral description and varying parameters);

wherein the program descriptions define the devices on a single bus by using a run method of the program language (Bowen, Col. 10, ll. 22-44,high-level language abstractions or models, wherein features include ability to define a bus);

wherein in the run method, program codes which are to be executed in a thread constituting a multi-thread are described (Bowen, Col. 25, ll. 44-52, wherein Handel-C is a parallel language allowing parallel thread implementation); and

8. Bowen does not disclose:

wherein the program language employed is a Java program language (Panchul, Java language); and

defining clock synchronizations of the device by using barrier synchronizations (Hines);

imposing an inhibition of dynamic instantiation restriction and an inhibition of a start method call from the run method restriction on the program descriptions by employing a Java program language;

wherein the intermediate expression is a member selected from the group consisting of a concurrent control flow flag, a temporal automaton with a concurrent parameter, and a temporal automaton with parameters;

wherein parametric model checking is performed for the parameter generation; and

wherein the real-time restriction is given by RPCTL.

9. Panchul discloses algorithmic representation of preliminary hardware design in high-level language such as Java (Panchul, Paragraphs 22, 112) with parallel processing of functions (Panchul, Paragraphs 62-63, 152).

10. Hines discloses defining clock synchronizations of devices by using barrier synchronizations (Hines, Paragraphs 255-261).

11. Curtis discloses development of a system wherein the rate of communication traffic within the system is controlled through imposing an inhibition of dynamic instantiation restriction and an inhibition of a start method call from the run method restriction on the program descriptions by employing a Java program language (Curtis, Paragraphs 20, 26, 44, 54-55, Figs. 4-5, “run ( )” method and “start ( )" method of “thread” objects).

12. Nakata discloses a symbolic model checking method for parametric periodic timed automata (Nakata, Abstract, Section 2, parametric and periodic timed automata) as a useful and effective method for reliable hardware/software system design (Nakata, Section 1, Introduction, first paragraph), wherein an algorithm is utilized for deriving parameters for a timed automaton model which satisfies a formula of a real-time extension of CTL (Nakata, Section 1, Introduction, fourth paragraph, Section 3, Real-time CTL).

13. It would have been obvious to one of ordinary skill in the art at the time of Applicant’s invention to substitute any standard C-type programming language such as Java, ANSI C, C++, etc. with the high-level language as taught by Bowen for flexibility amongst designers/programmers.

14. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate barrier synchronizations of Hines in order to enforce synchronization of activities (Hines, Paragraphs 255-261).

15. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention that incorporation of the inhibition of dynamic instantiation restrictions and inhibition of start method call from run method call restrictions in the Java programming language environment as taught by Curtis allows for a designed system to regulate activity and conserve execution time for other processes to run (Curtis, Paragraph 62).

16. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention that the teachings of Nakata for "on-the-fly" model checking used in the design of reliable hardware/software systems allows for reduction of computation complexity in model checking, thus providing time and processing power savings (Nakata, Section 1, introduction, fourth paragraph, Section 4.2, first paragraph, Section 5, first paragraph).

Remarks

17. The rejections of claims 1-4 and 6 under 35 U.S.C. 112, second paragraph have been removed in light of Applicant's amendment filed 5/19/2009.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick Sandoval whose telephone number is 571-272-

7973. The examiner can normally be reached on 8:00 am to 5:30 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Patrick Sandoval/

Examiner, Art Unit 2825

/Jack Chiang/

Supervisory Patent Examiner, Art Unit 2825